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Arrays of magnetic tunnelling junctions for field programmable logic gates

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Abstract

In spin-logic, one gains the advantages of magnetic film elements, i.e. non-volatility, the possibility of fast operation, radiation hardness and non-destructive readout. Here, we experimentally demonstrate the feasibility of logic gate arrays, based on spin-dependent tunnelling elements, which can be separately programmed on-chip to form a logic OR, AND, NOR or NAND function. Key factors for the tunnelling junctions and the gate arrays as reproducibility of both the resistance and the magnetoresistance, TMR amplitude and switching behaviour are discussed and demonstrated.

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Keywords: Magnetism; Tunnelling; Magnetoelectronic; Logic; Reconfigurable computing

1. Introduction

Spin-dependent tunnelling (SDT) elements are intensively studied due to their physical properties and possible application in sensors and memories. Additionally, programmable logic gates can be built by combining these elements with standard semiconductor components [1–3]. Because logic and programming operation in these gates are essentially the same, fast reconfigurable computing [4] can be performed with this logic device.

The feasibility of one concept [1] for a field programmable spin logic has been shown by realising a working three-input gate of six sub-micrometer SDT elements with a CoFe/Ru/CoFe artificial antiferromagnet (AAF) pinned by an antiferromagnetic IrMn layer [5].

In case of these fixed, i.e. non-programmable hard layers, an n-input field programmable spin-logic gate consists of $2n$ independently addressed SDT elements, arranged in two lines as shown by the SEM image in Fig. 1. The n SDT elements in a line are wired in series. In operation, tunnelling currents I_0 are applied to each line.

The logic output of the device is the voltage $U_{\mathrm{Out}} = I_0(R_1 - R_2)$, where R_1, R_2 are the tunnelling resistances of the two lines. The n logic inputs are formed by n SDT elements, the remaining SDT elements serve as reference bits.

2. Spin tunnelling junctions for logic gate arrays

For the function of these logic gate arrays, a large TMR amplitude and a low scattering of both TMR as well as the junction resistance is necessary in order to obtain a sufficient voltage gap in U_{Out} separating logic 1 from logic 0. Furthermore, independent switching of the elements with a combined clock- and input signal has to be achieved.

In Fig. 2, we show a TMR major loop which has an amplitude of 45%. If the other aforementioned conditions would be perfectly satisfied, this could give an output gap larger than 40 mV, which is enough for safe logic operation. The rms deviation of the typical TMR

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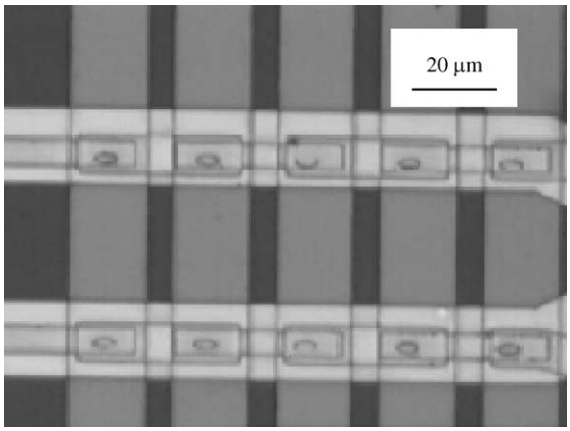

Fig. 1. SEM image of 10 SDT's, five of them in series as inputs and five in series as reference cells.

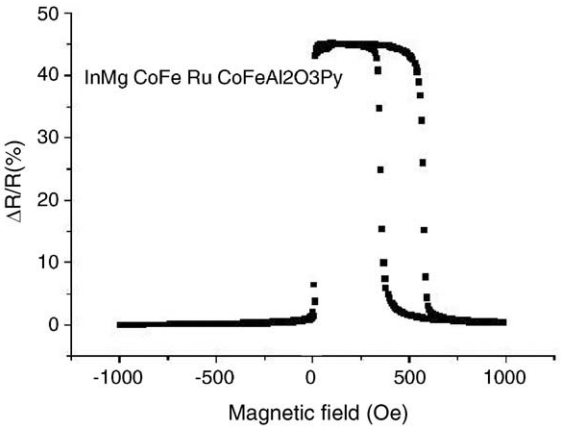

Fig. 2. TMR major loop of one tunnelling junction of the logic gate array with an amplitude of 48%.

amplitudes is only 1.7%. A more critical issue than TMR is the cell resistance due to its exponential dependence on the barrier thickness and on the square root of the barrier height.

Across a 4-in. Si-wafer, the spread of the resistance values is still not satisfying the needs of logic gate arrays. Within one gate, however, the resistance and—as shown in Table 1—also the coercive field, typically varies by about 2%.

Taking these deviations of TMR and resistance, typical gap values are between 30 and 40 mV, which still is a reasonable value for the operation of logic gate arrays.

The last point concerns the switching of the soft magnetic electrodes within one gate array, which is known to be a critical issue [6].

Table 1
Values for TMR amplitude, resistance and coercive field for five typical tunnelling junctions within one gate array

TMR (%)	$R(\Omega)$	H_c (Oe)
47.1	308	2.3
47.1	308	2.3
46.9	310	2.5
47.0	310	2.5
46.8	312	2.5

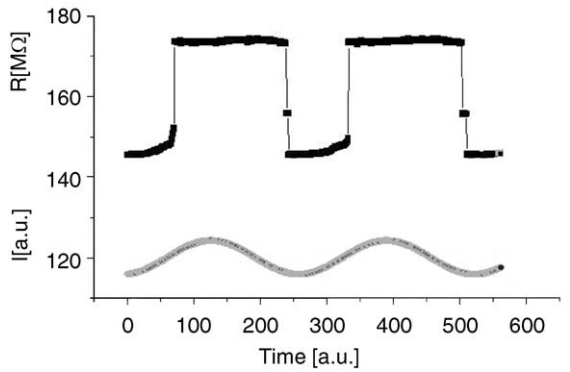

Fig. 3. Line current (grey) and resistance (black) of two tunnelling junctions in series. Only one of the junctions is switched by the line current.

In Fig. 3, we show the resistance of two elliptically shaped junctions in series and the current running through the switching line crossing one of them. A sharp minor loop switching can be observed with an amplitude of around 22%. This corresponds very well with the total TMR amplitude of around 45% for one junction, because for two SDT's the resistance is doubled referred to this value. Logic gate arrays thus can be successfully realised with these SDT's.

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