A GENERALIZED HSPICE[1] MACRO-MODEL FOR PSEUDO-SPIN-VALVE GMR MEMORY BITS

Bodhisattva Das and William C. Black, Jr.

Department of Electrical and Computer Engineering,
Iowa State University, Ames, Iowa 50011-3060.[2]

ABSTRACT

Nonvolatile semiconductor storage using Giant-Magneto-Resistance (GMR) memory bits has the potential for revolutionizing both high density and high speed memory applications with devices exhibiting unlimited write endurance and very low required write energy. This work presents the first generalized circuit macro-model for a *pseudo-spin-valve* GMR memory bit. The macro-model is realized as a four terminal sub-circuit which emulates GMR bit behavior over a wide range of sense and word line currents. The non-volatile and nonlinear nature of GMR memory bits are accurately represented by this model and simulations of non-volatile GMR latch structures with HSPICE show expected outcomes. The model is flexible and relatively simple: ranges of the write /read currents and bit resistance values are incorporated as parameterized variables and no semiconductor devices are used within the model.

1. INTRODUCTION

Since the first observation of the GMR effect in magnetic multilayers in 1988 [1], considerable research has been directed towards materials and structures that are capable of showing this phenomenon. GMR materials are now being used as highly sensitive magnetic sensors [2] and are responsible for a continued revolution in disk drive performance and storage density [3]. They also show promise of economical high density data storage in Magnetic Random Access Memory (MRAM) devices [4].

GMR devices employ two ferromagnetic layers separated by a very thin non-magnetic spacer layer. If properly fabricated the resistance of this composite structure is a significant function of the difference between the magnetic moments of the two layers. These layer magnetizations are themselves at least somewhat dependent upon the local magnetic field and typically have two or more stable magnetic states.

An interesting type of GMR device is popularly known as a *spin-valve* [5]. In this structure the magnetization of one ferromagnetic layer is pinned in one direction along the longitudinal direction of the stripe with a layer of anti-ferromagnetic material (such as MnO or MnFe). The magnetization of the other layer is free to rotate but as the bits become very narrow, it tends towards either a parallel or anti-parallel alignment relative to the pinned layer in reproducible and stable states [6]. These orientations correspond to the '0' or '1' states of the magnetic memory bit.

In a *pseudo-spin-valve* structure [7][8][9], neither magnetic layer is pinned but one layer (the "harder" one) has a higher switching field than the other. So, the application of a comparatively weak magnetic field can only alter the magnetic orientation of the "softer" layer, whereas a strong magnetic field can switch both layers.

For both spin-valve and pseudo-spin-valve structures when the pair of ferromagnetic layers are magnetized in the same (parallel) direction, the resistance of the stripe is lower than when they are magnetized in opposite (anti-parallel) directions. In this work, we model a pseudo-spin-valve GMR memory bit with a circuit macro-model that can easily be incorporated into HSPICE simulations. This work is an extension of the modeling of spin-valve bits done by us before [10], but is much more involved due to the complicated nature of pseudo-spin-valve bits. It is interesting to note that though there has been plethora of research on GMR materials or application circuits, we are not aware of any publication on simple circuit-models for pseudo-spin-valve GMR structures. *Our proposed model is thus apparently the first one for pseudo-spin-valve GMR bits.*

2. BEHAVIOR OF A GMR BIT

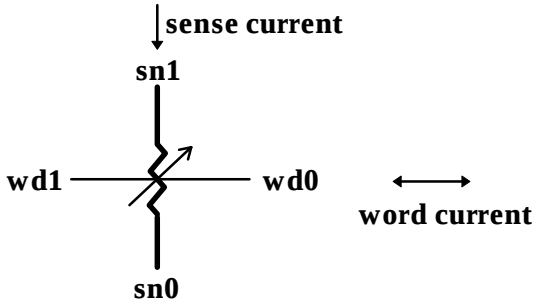

Figure 1. GMR bit with word line.

A GMR element can be considered as a four terminal device (Fig. 1). Two of the terminals connect directly to the GMR resistor (sense lines) while the other two provide a magnetic bias field for reading and writing of the bit (word lines). The word line and sense line are *not* connected to each other. A current through the word line induces a magnetic field on the GMR resistor which can change its resistance value. The effective value of the resistance is sensed between the two sense line terminals.

2.1 Pseudo-Spin-Valve Behavior

The resistance R vs. word current I_w graph of a typical pseudo-spin-valve GMR bit is shown in Fig. 2 [7][8][9]. The hysteretic nature of the graph can be easily observed: it is a combination of system N and system P. System N in turn can be divided into two

[1] HSPICE is an authorized trademark of Avant! Corporation.

[2] This work was sponsored in part by Solid-State Electronics Center of Honeywell Inc., Plymouth, MN; and DARPA.

graphs: Na and Nb (Fig. 3); similarly for P: Pa and Pb (Fig. 4). Ni's are points on system N and Pi's are points on system P. The R vs. I_w characteristic is symmetrical about a I_w=constant line through point C. For a conventional pseudo-spin-valve GMR, C is the zero-word-current point (I_{wc}=0); however, our macro model is flexible enough to handle a non-zero center point ($I_{wc}\neq 0$).

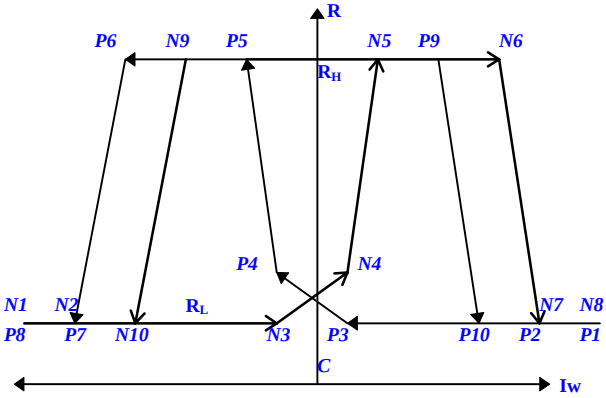

Figure 2. Pseudo-spin-valve R vs. I_w characteristic.

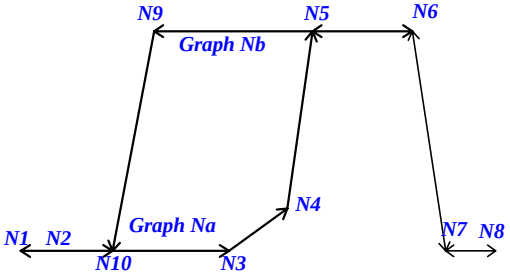

Figure 3. The System N characteristics: a combination of graphs Na and Nb.

If I_w is increased beyond N7 (which is the same as P2), the R vs. I_w characteristic gets onto the system P. Any subsequent magnetization caused by all word current values between points P2 (N7) and P7 (N2) will keep the R-I_w curve on system P only. If the word current value goes beyond point P7 (N2), the R-I_w curve changes its track and gets onto system N. Now, it will stay on system N for any values of word current between points N2 (P7) and N7 (P2). When we are on system N between points N5 and N6 (Figs. 2 & 3), and if now the word current is reduced before reaching N6, the characteristic does not retrace back to N3 via N5 and N4. Rather, the resistance stays high till a point N9 (somewhere between points P5 and P6) where it starts diminishing and finally reaches N10 and then goes back to N2 if the current is decreased (increased in the negative direction) further. Similarly, if we are on system P between points P5 and P6 (Figs. 2 & 4), and the current is increased (decreased in the negative direction) before reaching P6, the resistance stays high till a point P9 between N5 and N6. Then it starts falling down to point P10. So eventually each of the systems N and P can be conceived as a combination of two graphs. For system N, graph Na is called the *major loop* and graph Nb the *minor loop* (Fig. 3). Similarly for system P.

This hysteretic nature of the R vs. I_w characteristic makes the pseudo-spin-valve GMR useful as a memory element. We can arbitrarily assign state 0 to system N and state 1 to system P (or vice versa). When $I_w > I_{P2}$, we say that the GMR is "written" into state 1; and when $I_w < I_{N2}$, it is "written" into state 0. The GMR can be "read" at any word current between I_{N2} and I_{P2} ($I_{N2} \le I_w \le I_{P2}$) and the resistance sensed will depend on which state the GMR had been written into before.

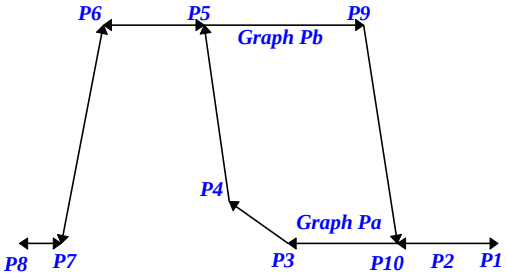

Figure 4. The System P characteristics: a combination of graphs Pa and Pb.

3. THE MACRO-MODEL

The proposed macro-model is conceived as a 4-terminal sub-circuit in HSPICE. Two of the four terminals (wd1 and wd0) are for the word line and the other two (sn1 and sn0) for the sense line (Fig. 1). The circuit can be divided into four simple parts:

1. input (word) circuit
2. bistable multivibrator or Schmitt Trigger
3. decision circuit
4. output (sense) circuit.

In Fig. 5, we annotate a part of the circuit: essentially the part that models system N.

3.1 Input (Word) Circuit

It comprises only one constant-value resistor R_w. The input word current I_w flows through R_w and creates a voltage proportional to I_w between nodes wd1 and wd0.

$$V(wd1,wd0) = R_w.I_w.$$

So, V(wd1, wd0) can be viewed as a scaled version of the word current itself.

3.2 Bistable Multivibrator or Schmitt Trigger

This circuit is realized (Fig. 5) as a very-high-gain (>>1) operational amplifier in a positive feedback configuration with the non-inverting output (node 4) fed back to the non-inverting input (node 5) through resistor R_2. The inverting input and output are shorted to wd0 point, and node wd1 is connected to the non-inverting input (node 5) via a resistor R_1. So, essentially, V(wd1, wd0) is fed to the non-inverting input (node 5) through R_1. The voltage difference between the differential outputs of the op-amp has upper saturation level V_{max} (L_+) and lower saturation level V_{min} (L_-). This circuit behaves as a bistable multivibrator depending on the value of V(wd1, wd0) [11]. In HSPICE this very-high-gain operational amplifier is realized by a Voltage Controlled Voltage Source (VCVS) named *Eopamp*. This bistable circuit has two stable voltage levels for node 4: L_+ and L_- [11]. As V(wd1,wd0) goes higher than $-L_-(R1/R2)$, the circuit regen-

erates and V(4) reaches upper stable state L_+. Similarly as $V(wd1,wd0) < -L_+(R1/R2)$, V(4) reaches lower stable state L_-.

In the entire macro-model, there are 3 bistable multivibrators: one for system N (to select between graphs Na and Nb), one for system P (to select between graphs Pa and Pb), and the third one for selecting between systems N and P.

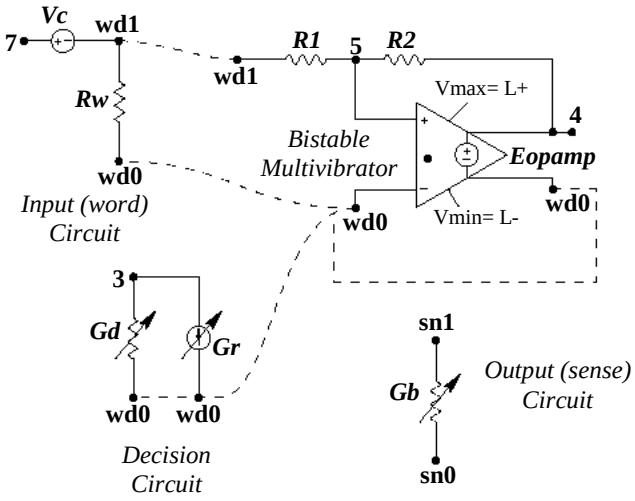

Figure 5. Part of the macro-model.

3.3 Decision Circuit

This circuit comprises G_d, a Voltage Controlled Resistor (VCR) and G_r, a Voltage Controlled Current Source (VCCS).

G_d is a VCR whose resistance is a one-to-one function of the controlling voltage V(wd1,wd0). More specifically, $R(G_d) = 1* V(7,wd0)$ where $V(7,wd0) = V(wd1,wd0) + V_c$; V_c being a constant voltage. So, V(7,wd0) is an origin-shifted version of V(wd1,wd0). *Ideally, we should have made* $G_d = V(wd1,wd0)$, but we cannot, because, HSPICE cannot handle any negative resistance. V_c is chosen to be a value such that V(7,wd0) never goes below zero and hence clipping of the 1:1 VCR characteristic of G_d at the negative region of the controlling voltage is avoided.

The VCCS G_r works as a unity magnitude current source, which has a value +1 or –1 depending on whether the Schmitt Trigger is at the upper stable level (L_+) or at the lower one (L_-). This current essentially creates a positive or negative voltage across G_d (between nodes 3 and wd0), based on the bistable state; i.e.,

$V(3,wd0) = V(7,wd0)$ if $V(4,wd0) = L_+$; and,

$V(3,wd0) = -V(7,wd0)$ if $V(4,wd0) = L_-$.

Once the characteristic is on system N, the current $I(G_r)$ governs which graph (Na or Nb) the GMR characteristic should take depending on the particular bistable state.

There is another similar group of V_c, G_d and G_r for system P. There is a switching circuit to select between systems N and P. The switching circuit is very simple (not shown in Fig. 5): two voltage controlled voltage sources (VCVS) having voltage values in 1:1 relation with the two V(3,wd0)'s; and two voltage controlled resistor (VCR) switches to select between them. The switches are complement to each other: they are ON/OFF depending on whether the third bistable multivibrator (the selector of the two systems) is at the high level or low level; the ON value of the VCRs being unity. The switched (selected) current is then passed through a unity resistor to generate the same voltage as V(3,wd0).

3.4 Output (Sense) Circuit

The sense circuit comprises a Voltage Controlled Resistor (VCR) G_b connected between sense line terminals (points sn1 and sn0). The resistance of G_b varies as a Piece-Wise Linear (PWL) function with the controlling voltage V(3,wd0). G_b is essentially the GMR bit; any external circuitry connected to sn1 and sn0 sees the resistance of G_b as the effective GMR resistance across the sense line terminals (between sn1 and sn0).

The R vs. I_w characteristic of the GMR is mapped into the PWL characteristic of G_b. We essentially have four different graphs (two N's and two P's) all varying between same boundary points and all of them have to be mapped into the same PWL of G_b. So we have to make sure that these four graphs are mapped into mutually-exclusive (non-coinciding) regions of the PWL function. Interestingly, the only modification that is needed to make the model suitable for different pseudo-spin-valve GMR structures is the PWL function of G_b: the entries for the controlling voltage and the resistance values have to be changed accordingly.

4. THE SPECIFIC CASE OF SYMMETRIC MAJOR AND MINOR LOOP

If we consider a simpler assumption that for system P (or N) the upward gradient of the major loop is symmetrical to the downward gradient of the minor loop, we have a characteristic which looks like Fig. 6. Here we can observe the points P9, P10, N9, N10 have different positions from the more generalized case of Fig. 2. Actually Fig. 6 is one particular case of Fig. 2. In this case, we can divide the characteristic into two curves: one for the actual top (*softer*) layer of GMR and the other for the actual bottom (*harder*) layer (Figs. 7 & 8). Then we can just combine the two curves (take absolute difference of the two and add to the nominal low value (R_L) of the GMR resistor) to obtain the Fig. 6 characteristic. This buys us a major advantage in terms of modeling: we can model the characteristic of Fig. 6 with only two bistable multivibrators, instead of the three we otherwise had for the more general case of Fig. 2.

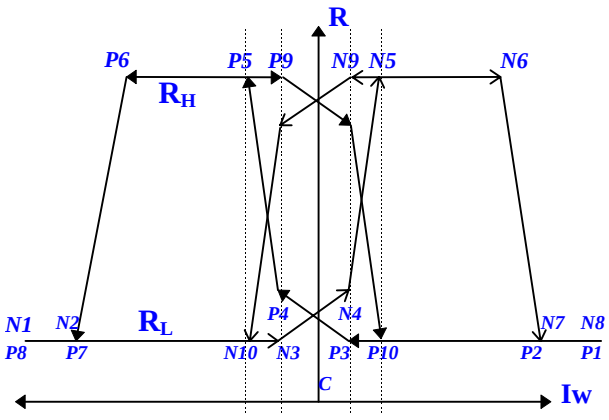

Figure 6. Symmetric major and minor loop.

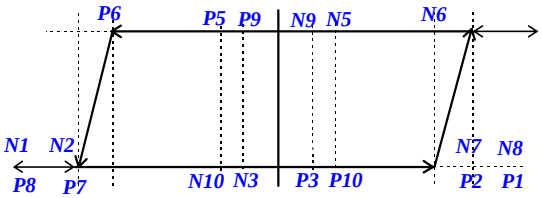

Figure 7. Bottom (*harder*) layer magnetization curve.

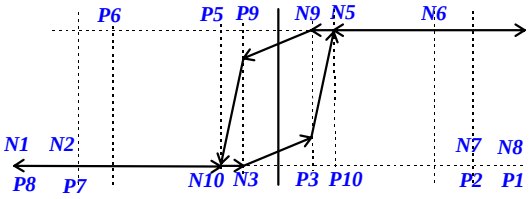

Figure 8. Top (*softer*) layer magnetization curve.

5. THE HSPICE NETLIST FILE

The simplicity of the macro-model and its compatibility with HSPICE format makes the task of writing a netlist file of the circuit very easy in HSPICE [12]. All the variables in the circuit can be written as .PARAM statements; hence they are all parameterized. The sub-circuit is not comprised of any component that needs a power supply, so its behavior is not influenced by any simulated power up or down. *This gives the model the non-volatile nature*. Moreover, there is no semiconductor device in the macro-model, hence possible complications due to different models for MOS or BJT devices is avoided. The entire sub-circuit is written as an HSPICE include file (*.inc).

6. SIMULATION

The GMR sub-circuit was simulated with HSPICE [12]. First a dc analysis was done for the GMR model only to verify that the model works fine for the whole range of word currents. Next, a transient analysis was done to verify that the model by itself has a proper transient response. One small limitation was detected. The node 5 in the bistable multivibrator sub-sub-circuit (Fig. 5) has to be initialized (once for all) to a small positive or negative voltage so that the bistable multivibrator can attain its positive or negative stable level. Otherwise, HSPICE doesn't understand what to do with the initial voltage at the node 5 and hence, keeps it at zero, eternally. This bottleneck was avoided by forcing a small voltage (positive or negative) as an initial condition (.IC statement) to node 5 in the macro-model itself. After this, the "acid test" of the macro model was done by replacing simple resistors with our GMR sub-circuit in a cross-coupled dynamic latch/sense-amplifier structure and simulating (transient) with HSPICE. After initial reset the latched states always showed the expected result. Also, the sub-circuit was put into novel pseudo-spin-valve GMR memory structures and simulated: the GMR bits showed proper state changes at write and read steps. The ΔR for the GMR bit was chosen to be 5% with R_L=100Ω and R_H=105Ω. The non-volatile nature of the GMR bit was also accurately demonstrated by the model.

7. CONCLUSION

To the authors' knowledge, this is the first published HSPICE model of a GMR bit for pseudo-spin-valve structures. This macro-model will be extremely useful for designers and researchers working on MRAM and in related fields. The flexibility of the model can be easily exploited by the users as they can customize this model by simply altering sub-circuit parameters. The simplicity of this model is a virtue, it doesn't use any of the published rigorously mathematical models of hysteresis [13][14].

8. REFERENCES

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