SA 17.5: Monolithic 4-20mA Isolating Current Replicator using GMR Resistors

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Electrical isolation devices are generally required in all circuits that employ multiple or distantly placed grounds, in virtually all medical devices that electrically contact the human body, and in many power-control applications. Isolation circuits invariably use some form of complex or hybrid packaging and either opto-isolators or rate-sensitive isolation elements such as capacitors or transformers [1]. Opto-isolators are intrinsically non-monolithic while capacitors and transformers require that dc and low-frequency signals be converted into ac before being passed through the isolation device and then converted back into its original state [2]. With any of these techniques, it is not practical to fully integrate the isolation devices with other circuitry or other isolation devices. Furthermore, the isolators themselves are often slow or awkward to interface to other circuitry. The technique demonstrated here overcomes these drawbacks with the simple addition of a few thin film and insulator depositions steps to a standard integrated circuit process. This allows for the first time, truly isolated inputs and even multiple isolated inputs on an otherwise conventional bipolar or CMOS process at low cost.

This circuit is an isolated current replicator that produces an output current that closely matches that present in an isolated input current loop. Typical uses of this circuit would be as an isolated receiver of 4-20mA transducer data or in a traditional isolation amplifier. This device uses four magnetic field sensitive resistors in a bridge configuration in conjunction with two on-chip current loops and a conventional bipolar operational amplifier. The resistive sensors employ giant magnetoresistive ratio (GMR) material that displays a high magnetic sensitivity and is easily incorporated into a conventional integrated circuit process [3, 4]. GMR films consist of stacks of 2 or more magnetic layers separated by thin non-magnetic intermediate layers such as copper. The resistance can be decreased by as much as 5-6% by applying a magnetic field of up to about 50Oe. The magnetic field is provided by a current-carrying wire placed over the resistors. Each of the two current loops is connected diagonally across resistors on opposite corners of the bridge so that any difference between the two loop currents is reflected as a bridge imbalance which is then presented to the amplifier [5]. One of the input loops contains the isolated and unknown current to be sensed while the other contains a counterbalancing feedback current from the on-chip amplifier (Figure 1). The amplifier serves to balance the bridge by providing a feedback current equal to that present in the isolated current input line. This topology has several advantages; the overall circuit response is linear despite significantly nonlinear GMR characteristics and the required common-mode input and output voltage range of the amplifier is small.

The current loops are conventional aluminum lines that are electrically isolated from the resistive sensors by a thick layer of silicon-nitride. Provided minimum geometry and spacing rules are followed, multiple isolator circuits may be placed on a single integrated circuit with each having an isolated input current loop.

A micrograph of the integrated GMR isolator is shown in Figure 2. The 7-turn current loops produce approximately 1Oe/mA loop current at the GMR resistors. A plasma enhanced chemical vapor deposition (PECVD) process is used to deposit a 2.5μm thick Si3N4 insulation barrier between the sandwich film and the Al coils. The total input loop impedance is about 37Ω and the GMR resistors are about 1.7kΩ each. A schematic of the bipolar amplifier used for generating the feedback current is shown in Figure 3. A 741 type input stage (Q1-Q6) provides good common-mode rejection and reduces the size of the required compensation capacitor, which is a large-area junction capacitor (Q13). This type of input stage may be used even with a 5V supply because of the limited common-mode input range of the application. Additional broadbanding is provided by diffused resistor R1 in series with Q13. The relatively high current output stage is provided by a Darlington npn pair for driving the on-chip feedback coil (Q11 and Q12). This stacked transistor arrangement is possible on a 5V supply because of the limited output voltage range required. Amplifier biasing is by a supply-independent reference composed of Q14 - Q20 and R3 and R4. A long JFET provides start-up current. A summary of measured isolator performance is presented in Table 1.

Untrimmed GMR bridges show a typical output offset voltage of about .5 % of Vcc which corresponds to an equivalent input current offset of about 5 mA in this current replicator circuit. In the parts tested, this offset is trimmed with a simple 1-point offset adjust of the bridge output. This trimming is by an external 100kΩ trimpot between the bridge outputs and ground. Conventional laser trimming could be used on the GMR resistors themselves, which are optically opaque and easy to evaporate with low beam energy. Packaging related effects are minimized by designing the GMR films to be minimally magnetostrictive.

A measured dc transfer characteristic of the isolator taken at wafer probe with an HP4155A parameter analyzer is shown in Figure 4 along with nonlinearity about the best-fit line (in % of full scale). Digitized oscilloscope images of isolator performance are presented in Figures 5 and 6 using an external 100Ω current sense resistor in series with the feedback current loop. Figure 5 shows ramp performance with a 5-15mA 10kHz triangle wave input while Figure 6 demonstrates common-mode rejection performance. In the latter case, an 80V peak-to-peak common-mode signal applied to the isolator input produces about a 50μA error current in the 10mA dc signal current. Wafer-level tests of isolation breakdown characteristics showed no failures up to the 800V limit set by probe card surface plasma effects.

Acknowledgments:

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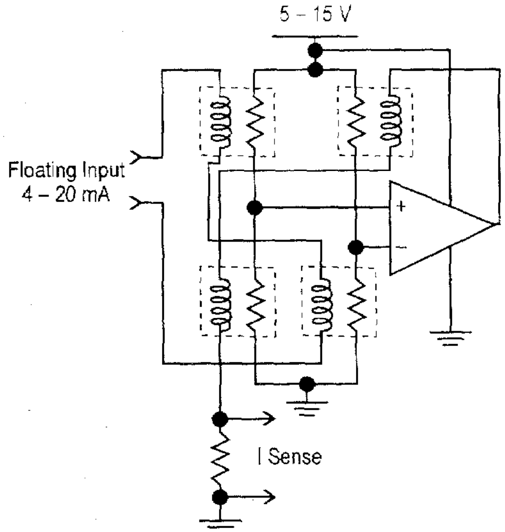

Figure 1: Isolation circuit schematic diagram.

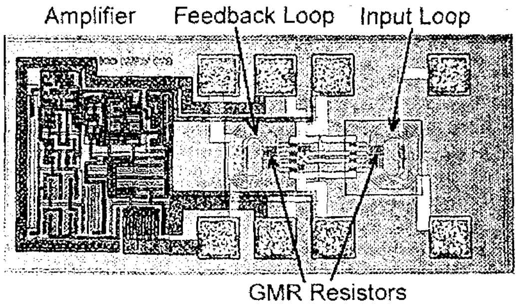

Figure 2: Die micrograph (.72 mmx1.5 mm).

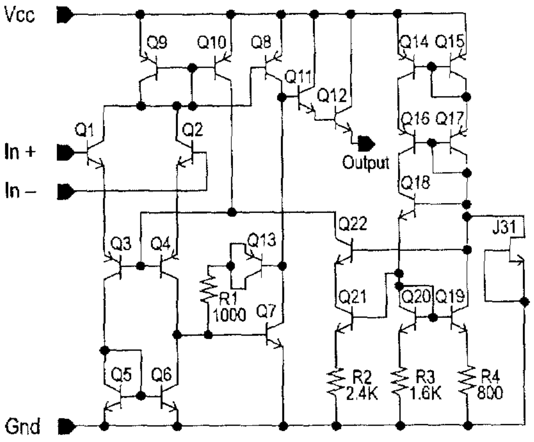

Figure 3: Amplifier schematic.

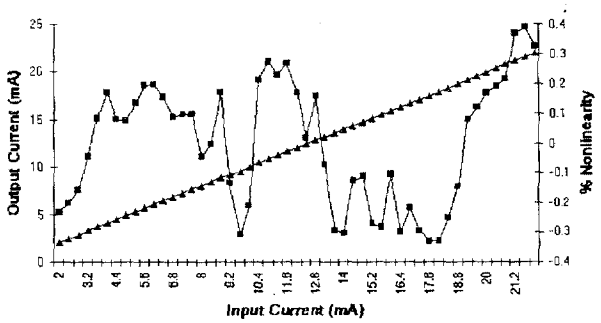

Figure 4: Measured isolator nonlinearity.

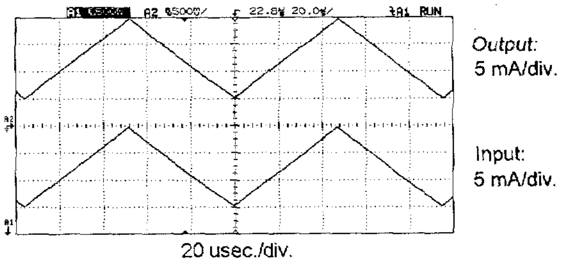

Figure 5: 5-20mA ramp at Vcc = 5V.

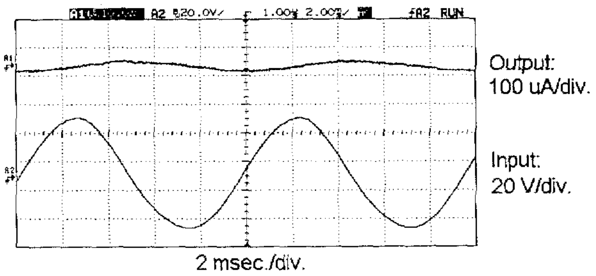

Figure 6: CMRR at dc input = 10mA and Vcc = 5V.

Power Dissipation (Iout = 4 mA)	53	mW
Error from best-fit line after single point offset trim (4-20 mA range)	< .5	% of full scale
Gain Error	< 1.5	%
Untrimmed Equiv. Offset	5	mA
- 3dB Bandwidth	DC - 400	kHz
Max. Slew Rate	20	mA/usec.
± 10mA Settling Time (.1%)	< 2	µsec.
Isolation Voltage	> 800*	Volts
Die Size	.72 x 1.5	mm

*limited by wafer probe setup

Table 1: Summary of isolator characteristics at Vcc = 5v.